1. (Cancelled)

2. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle.

3. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device and each has an area for connection of a single bonding wire.

4. (Previously Presented) The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times of a height of the semiconductor die.

5. (Previously Presented) The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device.

6. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals each represent a local deformation of the carrier device which is formed by a punch or a bending-off device.

7. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals are formed by application of material to the carrier device.

8. (Previously Presented) The integrated circuit of claim 16, wherein a silver or gold finish is applied to the stamped pedestals.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Previously Presented) The integrated circuit of claim 17, where the stamped pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls, with the sidewalls having rounded junctions parallel to the plane of the carrier device or being rounded as a whole.

14. (Previously Presented) The integrated circuit of claim 17, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height itself.

15. (Previously Presented) The integrated circuit of claim 16, where only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.

16. (Currently Amended) An integrated circuit, comprising:

a semiconductor die;

a carrier device comprising a die paddle onto which the die is attached ~~and a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion~~, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion;

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion; and

a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

17. (Currently Amended) An integrated circuit, comprising:

a semiconductor die;

a metallic carrier device comprising a planar surface onto which the die is attached ~~and a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion~~, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion; and

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion.

18. (Withdrawn) An integrated circuit, comprising:

a non-conductive carrier device having a plurality of integrally raised pedestals, at least one of the pedestals having a bonding pad;

a semiconductor die coupled to the non-conductive carrier device, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure; and

a first bonding wire electrically coupling the semiconductor die to the bonding pad.

19. (Withdrawn) The integrated circuit of claim 18, further comprising

a lead; and

a second bonding wire electrically coupling the bonding pad to the lead.

20. (Withdrawn) The integrated circuit of claim 19, further comprising a package that encapsulates the semiconductor die, the first and the second bonding wires and a portion of the lead.

21. (Withdrawn) The integrated circuit of claim 18, wherein the bonding pad is composed of at least one of gold and silver.

22. (New) The integrated circuit of claim 16, where a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device.

23. (New) The integrated circuit of claim 17, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device.

24. (New) The integrated circuit of claim 16, where the metallic leads are separate from the carrier device.

25. (New) The integrated circuit of claim 17, where the metallic leads are separate from the metallic carrier device.